Abstracts

Unaided 2.5 Gb/s silicon bipolar clock and data recovery IC

G. Gutierrez and Shyang Kong. "Unaided 2.5 Gb/s silicon bipolar clock and data recovery IC." 1998 Radio Frequency Integrated Circuits (RFIC) Symposium 98. (1998 [RFIC]): 173-176.

We will describe a low cost and low power Si Bipolar IC for clock and data recovery at 2.488 Gb/s that requires no external reference. The design is based on a digital quadri-correlator that has inherent low phase offset and allows the use of passive loop filters. The clock recovery unit (CRU) has broad locking range that makes it robust against power supply and temperature variations.

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